PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-006805

(43)Date of publication of application : 14.01.1993

(51)Int.Cl. H01C 7/10

(21)Application number : 03-183823

(22)Date of filing : 27.06.1991

(71)Applicant : MURATA MFG CO LTD

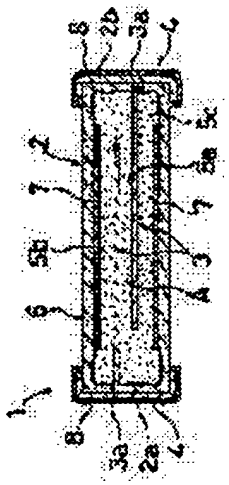
(72)Inventor : NAKAMURA KAZUYOSHI
UENO YASUSHI
NAKAYAMA AKIYOSHI
YONEDA YASUNOBU

(54) CHIP-TYPE VARISTOR

(57)Abstract:

PURPOSE: To provide a chip-type varistor which can have a glass film of the uniform thickness formed on the surface of a ceramic body that prevents the glass film from being diffused into an internal electrode for avoiding the deterioration in electric characteristic.

CONSTITUTION: The plurality of internal electrodes 3 are buried in a ceramic body 2 and one end face 3a of each internal electrode 3 is connected to an internal electrode 4 which is formed on left and right end faces 2a, 2b of the ceramic body 2. Then, the outer surface of the ceramic body 2 is coated with a glass film 6. Thus, a chip-type varistor 1 is fabricated. Between the surface of the ceramic body 2 and the internal electrode 3, a free electrode 7 not connected to the external electrode 4 is installed. An area of the free electrode 7 is made larger than that of a characteristic part A of the internal electrode 3 so that the free electrode 7 may cover the characteristic part A. For the free electrode 7, a silver-palladium alloy or platinum is employed.



LEGAL STATUS

[Date of request for examination]	16.03.1998
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3008567
[Date of registration]	03.12.1999
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] The chip mold varistor characterized by to arrange the free electrode which is not connected to the above-mentioned external electrode between the surface part of the above-mentioned sintered compact, and an internal electrode at the outside surface of the above-mentioned sintered compact in the chip mold varistor which comes to carry out covering formation of the glass membrane while laying two or more internal electrodes under the interior of a ceramic sintered compact and connecting the end side of this internal electrode to the external electrode formed in the end face of the above-mentioned sintered compact.
[Claim 2] The chip mold varistor characterized by the above-mentioned free electrode being larger than the area of the property section which discovers the voltage ratio linear characteristic in an internal electrode, and having covered this property section in claim 1.
[Claim 3] The chip mold varistor characterized by the above-mentioned free electrode consisting of a silver-palladium alloy or platinum in claim 1 or 2.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Industrial Application] This invention relates to the structure which controls the diffusion to an internal electrode and enabled it to prevent aggravation of an electrical property while being able to equalize the thickness of this glass membrane in the case of carrying out covering formation of the glass membrane especially on the surface of a sintered compact about the chip mold varistor which functions as an electrical-potential-difference nonlinear resistor.
[0002]
[Description of the Prior Art] In recent years, in the field of the electronic equipment adopted as a transmitter etc., a miniaturization and integration are progressing quickly. Moreover, reduction-ization of the withstand voltage by the densification of IC is demanded, and the protection component and circuit design for preventing the destruction and malfunction of IC circuit by invasion of a high-voltage nature noise in connection with this are needed. The varistor which has electrical-potential-difference non-linear characteristics as such a protection component is adopted. In order to apply this varistor to IC circuit, conditions, such as that a control electrical potential difference is low, that electrostatic capacity is small, and a still smaller thing, are required. However, in the above-mentioned varistor, since voltage at reference current must be lowered to lowering a control electrical potential difference, there is a problem that electrostatic capacity becomes large. Moreover, although it is possible by making an electrode surface product small to lower electrostatic capacity, when it does in this way, there is a problem that a surge tolerated dose falls. The chip varistor of a laminating mold is conventionally proposed as what can respond to a miniaturization, reducing such a control electrical potential difference and electrostatic capacity (for example, refer to JP,58-23921,B). . This laminating mold varistor carries out the laminating of a semiconductive-ceramics layer and the internal electrode by turns, really sinters them, exposes the end side of the above-mentioned internal electrode to the both-ends side of this sintered compact, forms the external electrode connected to this both-ends side in the end side of the above-mentioned internal electrode, and is constituted. By the way, although the above-mentioned chip varistor is useful as a noise absorption component, when size of this varistor component is made small, there is a problem of being easy to produce surface current and the leakage current by surface discharge. Moreover, since Ag is used for the above-mentioned external electrode, in case a surface mount is carried out by soldering, there is a problem of being easy to produce solder ******. In order to avoid such the leakage current and solder ******, it is effective to coat and insulation-ize glass membrane to the outside surface except the external electrode of a sintered compact. As an approach of coating this glass membrane, the method of the above-mentioned glass being burned at the temperature of 400 - 900 **, and making the surface part of a sintered compact diffuse this glass is adopted conventionally. While being able to control the leakage current by forming this glass membrane, the plating film by electrolytic plating can be covered on the front face of an external electrode, and solder ****** can be prevented. Here, when covering the plating film to the above-mentioned external electrode, since the above-mentioned sintered compact is a semi-conductor, if the front face of this sintered compact is not

insulation-ized certainly, it has a possibility that plating may grow up to be the whole front face, and may short-circuit, or the depressor effect of the leakage current may decrease. Therefore, it needs to equalize this thickness, therefore sets up the baking temperature of the above-mentioned glass highly, and is made to enlarge surface diffusion while a certain amount of thickness is required for the above-mentioned glass membrane.

[0003]

[Problem(s) to be Solved by the Invention] However, in the above-mentioned conventional chip varistor, when baking temperature of glass is made high, it may become active, this glass may attain even an internal electrode, as a result, voltage at reference current and a control electrical potential difference rise, and the grain boundary diffusion of glass also has the trouble of having a bad influence on a varistor property. In order to avoid the diffusion to an internal electrode here, making thickness of glass membrane into homogeneity, it is possible a glass content and by being burned and controlling temperature delicately. However, this control is very difficult and difficult in the present condition. It aims at offering the chip mold varistor which this invention was made in view of the above-mentioned conventional situation, and it can equalize thickness, being burned in the case of forming glass membrane on the surface of a sintered compact, and making delicate control of temperature unnecessary, and controls the diffusion to an internal electrode, and can prevent the bad influence to a varistor property.

[0004]

[Means for Solving the Problem] Then, invention of claim 1 lays two or more internal electrodes under the interior of a sintered compact, and it is characterized by to arrange the free electrode which is not connected to the above-mentioned external electrode between the surface part of the above-mentioned sintered compact, and an internal electrode at the outside surface of the above-mentioned sintered compact in the chip mold varistor which comes to carry out covering formation of the glass membrane while it connects this internal electrode to the external electrode formed in the both-ends side of the above-mentioned sintered compact. Moreover, the above-mentioned free electrode of invention of claim 2 is larger than the area of the property section in an internal electrode, and it is characterized by having covered this property section, and claim 3 is further characterized by the above-mentioned free electrode consisting of an Ag-Pd alloy or Pt.

[0005]

[Function] According to the chip mold varistor concerning invention of claim 1, since the free electrode was arranged between the surface part of a sintered compact, and the internal electrode, this free electrode will control diffusion inside glass, therefore even if it can be burned and sets up temperature highly, the diffusion to an internal electrode can be reduced, and aggravation of a varistor property can be avoided. Consequently, being burned and making delicate control of temperature unnecessary, thickly [thickness], uniform glass membrane can be formed and insulation can be improved. Moreover, in invention of claim 2, since the free electrode was made larger than the area of the property section of an internal electrode, diffusion of the glass to an internal electrode can be controlled still more certainly. Furthermore, by invention of claim 3, since a silver-palladium alloy and platinum were adopted as the free electrode, the depressor effect of diffusion of glass can be improved.

[0006]

[Example] Hereafter, the example of this invention is explained about drawing. Drawing 1 thru/or drawing 4 are drawings for explaining the chip mold varistor by one example of this invention. While laying underground the internal electrodes 3 and 3 of a pair which 1 is the chip mold varistor of this example in drawing, and become the interior of the sintered compact 2 of the shape of a rectangular parallelepiped which consists of semiconductive ceramics with which this uses ZnO as a principal component from an Ag-Pd alloy, it is the left of this sintered compact 2, The external electrode 4 which becomes right end side 2a and 2b from Ag is formed, and it is constituted. End side 3a of each above-mentioned internal electrode 3 is the left of the above-mentioned sintered compact 2, It exposes to right end side 2a and 2b by turns, and connects with the above-mentioned external electrode 4, and other end faces are enclosed in the sintered compact 2. Moreover, nickel plating film 8 by electrolytic plating is

covered by the outside surface of the above-mentioned external electrode 4.
[0007] Moreover, the ceramic layer 5a part pinched with both the internal electrodes 3 of the above-mentioned sintered compact 2 serves as the property section A which discovers electrical-potential-difference non-linear characteristics, and this property section A serves as an opposed face of both the above-mentioned internal electrodes 3. Moreover, parts other than ceramic layer 5a of the above-mentioned sintered compact 2 serve as the ceramic layers 5b and 5c as a dummy.
[0008] Furthermore, glass membrane 6 is formed in the outside surface of the above-mentioned sintered compact 2, and this glass membrane 6 makes the surface part of a sintered compact 2 diffuse HOU lead silicate system glass powder by the ability being burned at an elevated temperature, and is formed.
[0009] And in ceramic layer 5b between the internal electrode 3 of the above-mentioned sintered compact 2, and a front face, and 5c, the free electrode 7 which consists of an Ag-Pd alloy which is not connected to the external electrode 4 is arranged, and this free electrode 7 is enclosed in the sintered compact 2. Moreover, this free electrode 7 is set up more greatly than the area of the property section A of the above-mentioned internal electrode 3, and has covered this property section A. Diffusion inside the above-mentioned glass layer 7 is controlled with this free electrode 7.
[0010] Next, the manufacture approach of the chip mold varistor 1 of this example is explained. first -- as a ceramic raw material -- ZnO of 99% or more of purity, Bi 2O3, CoCO3, MnO2, and Sb 2O3 98mol %, 0.5mol %, 0.5mol %, 0.5mol %, and 0.5 mol % come out comparatively, respectively, weighing capacity is carried out, pure water is added to this, it mixes with a ball mill for 24 hours, and a slurry is formed. Next, after carrying out filtration desiccation and coming this slurry, temporary baking is carried out at the temperature of 800 degrees C for 2 hours. Then, after adding pure water to this, pulverizing by BORUMIRU, after carrying out coarse grinding of this baking object with a pulverizer, and carrying out filtration desiccation of this, with an organic binder, it distributes in a solvent and a slurry is formed. this slurry to a doctor blade method -- 50 micrometers in thickness a green sheet -- forming -- this green sheet -- the magnitude of a predetermined dimension -- piercing -- many -- the ceramic sheet of several sheets is formed. Ceramic layer 5a which discovers electrical-potential-difference non-linear characteristics by this, and the ceramic layers 5b and 5c as a dummy are formed.
[0011] Next, the conductive paste which consists of an Ag-Pd alloy (7:3 comparatively) is created, this paste is screen-stenciled on the top face of the above-mentioned ceramic layers 5a and 5c, and an internal electrode 3 is formed. In this case, it forms so that only end side 3a of an internal electrode 3 may be located in the rim of the ceramic layers 5a and 5c and the remaining end face may be located inside the ceramic layers 5a and 5c. Moreover, similarly conductive paste is printed on the top face of another ceramic layers 5b and 5c, and the free electrode 7 is formed in it. All the end faces of this are located inside the periphery of the ceramic layers 5b and 5c, and this free electrode 7 is formed so that it may become larger than the area of the property section A of the above-mentioned internal electrode 3.
[0012] Subsequently, end side 3a of each internal electrode 3 is the left so that each internal electrode 3 may counter on both sides of ceramic layer 5a, as shown in drawing 4 , It piles up so that it may be alternately located in the right, and the ceramic layers 5b and 5c which are not printed at all by the top face of this and the inferior surface of tongue are piled up two sheets. While piling up the ceramic layers 5b and 5c by which the free electrode 7 was furthermore formed in the top face of this, and the inferior surface of tongue, the ceramic layers 5b and 5c which are not printed at all are piled up two sheets. Next, the pressure of 2 t/cm2 is applied and stuck in the direction of a laminating of this by pressure, and this forms a layered product. Then, after cutting a layered product in a predetermined dimension, heating this at the temperature of 500 degrees C for 2 hours and vanishing a binder, a temperature up is carried out to 950 **, it calcinates for 2 hours, and a sintered compact 2 is obtained.
[0013] Thus, while holding the obtained sintered compact 2 in an alumina-ceramics pot, with a total weight [of the above-mentioned sintered compact / 1wt% of] HOU lead silicate system glass powder is added in this pot. And it heats to 700 - 900 **, rotating the above-mentioned porcelain pot. Then, the above-mentioned glass powder is spread into the surface part of a sintered compact 2, and, thereby, glass membrane 6 is formed. In this case, diffusion inside is prevented with the free electrode 8, osmosis in an internal electrode 3 will be controlled, and, as for glass powder, the glass membrane 6 of uniform

thickness is formed in the surface part of a sintered compact 2.
[0014] Next, left where end side 3a of an internal electrode 3 of the above-mentioned sintered compact 2 was exposed, After applying Ag paste to right end side 2a and 2b, it heats for 10 minutes by 800 **, and the external electrode 4 is formed. After an appropriate time, electrolytic plating is performed to the above-mentioned sintered compact 2, and nickel plating film 8 is formed in the outside surface of the above-mentioned external electrode 4. In this case, since parts other than external electrode 4 of the above-mentioned sintered compact 2 are covered by glass membrane 6, plating does not adhere. Thereby, the chip mold varistor 1 of this example is manufactured.
[0015] Thus, since according to this example the free electrode 7 was arranged between the front face of a sintered compact 2, and the internal electrode 3 and the property section A of the above-mentioned internal electrode 3 was covered with this free electrode 7, diffusion of glass can be controlled with the free electrode 7, the diffusion to an internal electrode 3 is reduced, and the rise of discharge voltage and voltage at reference current can be avoided. Moreover, while being able to reduce the leakage current, without the tension of the fused glass being able to become small, being able to improve the wettability to a component, and being able to form the uniform glass membrane 6 thickly [thickness], consequently spoiling a surge tolerated dose and electrical-potential-difference depressor effect from the ability of temperature for it being burned and being made high, solder ****** at the time of soldering can be prevented. In addition, although the above-mentioned example explained taking the case of the structure which laid the internal electrode 3 of a pair underground in the sintered compact 2, this invention is not restricted to this and can be applied also to the thing of structure which laid many internal electrodes underground.
[0016]
[Table 1]

試料No.	電極材料	フリー電極パターン	Δt (mm)	ガラス熱処理温度 (℃)	バリスタ電圧 V_{1mA} (V)	非直線係数 α	静電容量 C (pF)	誘電損失 tan δ (%)	制限電圧比 V_{2A}/V_{1mA}	半田付 V_{1mA} 変化率 加工変化 (%)	電解Niメッキ後 V_{1mA} (V)	150 Aサージ 変化率 ΔV_{1mA} (%)
1	Ag－Pd	なし	—	—	34.2	34	242	4.6	1.42	−63	Short	−10.7
2	↓	〃	—	700	34.1	34	243	4.7	1.43	−42	Short	−8.5
3	↓	〃	—	750	34.6	33	238	3.6	1.42	−39	Short	−9.1
4	↓	〃	—	800	35.0	31	216	2.6	1.45	−15	Short	−9.6
5	↓	〃	—	850	35.4	28	187	2.5	1.52	−10	35.3	−15.6
6	↓	〃	—	900	36.1	26	169	2.1	1.61	−5	36.1	−23.4
7	↓	b	0.2	850	34.9	28	192	2.8	1.45	−12	34.7	−8.6
8	↓	b	0.1	↓	34.6	28	201	3.0	1.45	−10	34.6	−6.5
9	↓	a	0.0	↓	34.4	30	225	3.1	1.42	−4	34.2	−2.4
10	↓	a	0.1	↓	34.4	33	235	2.9	1.41	−2	34.5	−1.8
11	↓	a	0.2	↓	34.3	34	244	3.0	1.42	−3	34.2	−1.5
12	↓	a	0.4	↓	34.2	34	246	3.2	1.41	−3	34.1	−1.6
13	↓	b	0.2	900	35.4	27	182	2.6	1.54	−9	35.5	−17.6
14	↓	b	0.1	↓	35.2	28	196	2.8	1.50	−6	35.3	−11.2
15	↓	a	0.0	↓	34.8	30	216	3.0	1.47	−4	34.6	−4.8
16	↓	a	0.1	↓	34.6	33	229	3.0	1.44	−3	34.4	−1.6
17	↓	a	0.2	↓	34.5	33	243	2.9	1.42	−4	34.5	−0.8
18	↓	a	0.4	↓	34.3	34	241	3.1	1.42	−2	34.3	−0.3
19	Pt	a	0.2	850	34.4	35	239	2.7	1.40	−3	34.4	−1.7
20	↓	a	↓	900	34.5	33	241	2.9	1.40	−2	34.4	−1.5

[0017] Table 1 shows the test result which checks the effectiveness of the chip mold varistor of this example and which went to accumulate. This trial created many chip mold varistors by the manufacture approach of the above-mentioned example, and measured the voltage at reference current at the time of changing the area of the free electrode in each of this varistor, a nonlinear multiplier, electrostatic capacity, electrostatic loss, a clamping voltage ratio, soldering processing rate of change, the voltage at reference current after plating, and surge rate of change, respectively. Moreover, as the above-mentioned

free electrode is shown in drawing 5 , property aspect product t1xt2 of an internal electrode are received (refer to drawing 5 (c)). When area of a free electrode was enlarged within the limits of t1+deltat and t2+deltat (0-0.4mm) (refer to drawing 5 (a)), and when area of a free electrode was made small within the limits of t1-deltat and t2-deltat (0.1 to 0.2 mm), it followed (refer to drawing 5 (b)). Here, to each sample after external electrode formation, the above-mentioned soldering processing rate of change was immersed in the 4x6 solder tub of 860 ** for 5 seconds using the rosin, after washing for 60 seconds by trichloroethane after this, was left for 1 hour and measured. Moreover, a clamping voltage ratio is 8x20microsec. It is the ratio of the output voltage/voltage at reference current when impressing a triangular current wave, and surge rate of change is the voltage at reference current/rate of the front [impression] varistor change of potential when leaving it for 1 hour, after impressing the above-mentioned triangular current wave. In addition, in order to compare, measurement with the same said of the conventional chip varistor which is not arranging the free electrode was carried out. Although it can be conventionally satisfied with a sample (No.1-6) of voltage at reference current and a nonlinear multiplier when [with glass baking temperature as low as 700 - 800 **] there is no free electrode so that clearly also from Table 1, in dielectric loss and soldering processing rate of change, it is low, and further, it adhered on the surface of [whole] the sintered compact, and short-circuits in plating processing, and the thickness of glass membrane serves as an ununiformity. Moreover, although it can be burned, and glass membrane is homogeneity when temperature is as high as more than 850 **, voltage at reference current and a nonlinear multiplier have deteriorated, and glass is spread even in the internal electrode. voltage at reference current on the other hand since glass turned around the free electrode and is spread inside, when the area of the above-mentioned free electrode is smaller than the property section of an internal electrode (sample No.7, 8, 13, 14), and a ratio -- in properties, such as a straight-line multiplier, effectiveness is small a little. On the other hand, the property which can be satisfied in soldering processing rate of change, the voltage at reference current after plating, and all the surge rate of change is acquired, without each spoiling each property of voltage at reference current, a nonlinear multiplier and dielectric loss, and a clamping voltage ratio, when area of a free electrode is made larger than the property section (sample No.9-12, 15-20).

[0018]

[Table 2]

試料No.	ガラス焼付温度（℃）	x軸（μm）	y軸（μm）
2	700	20	15
3	750	40	30
4	800	100	70
5	850	200	150
6	900	350	250

[0019]

[Table 3]

試料No.	ガラス焼付温度（℃）	x軸（μm）	y軸（μm）
11	850	130	150
17	900	170	250

[0020] Table 2 and 3 elects a sample (No.2-6) and this example sample (No.11, 17) which arranged the free electrode conventionally which is not arranging the free electrode adopted as the above-mentioned trial, carries out cross-section polish of each sample, and shows the result of having investigated the diffusion length of the glass of this by the electron probe X-ray microanalyser (energy dispersion mold). This measured the diffusion length in the direction x axis of a laminating of a sintered compact 2, and the diffusion length in the rectangular direction y-axis of this laminating direction, as shown in drawing 2 . In addition, the distance from the front face of the sintered compact 2 in each above-mentioned sample to the free electrode 7 is 100. mum, The distance from a free electrode to an internal electrode is 100. mum Carrying out [and], the distance from the side edge side of a sintered compact to the side edge side of an internal electrode is 400. mum It carried out. If baking temperature required for insulation-izing by the sample without a free electrode is made into 850 **, glass has reached even the property section of an internal electrode conventionally, so that clearly also from each table. On the other hand, it turns out that glass did not reach an internal electrode even if it could be burned and raised temperature by this example sample to 900 **, but the free electrode has controlled diffusion inside glass.

[0021]

[Effect of the Invention] Since the free electrode which is not connected to an external electrode was arranged between the surface part of a sintered compact, and the internal electrode according to the chip mold varistor which starts this invention as mentioned above, it is effective in being able to equalize thickness, being burned in the case of forming glass membrane on the surface of a sintered compact, and making delicate control of temperature unnecessary, and controlling the diffusion to an internal electrode, and being able to prevent the bad influence to a varistor property.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Industrial Application] This invention relates to the structure which controls the diffusion to an internal electrode and enabled it to prevent aggravation of an electrical property while being able to equalize the thickness of this glass membrane in the case of carrying out covering formation of the glass membrane especially on the surface of a sintered compact about the chip mold varistor which functions as an electrical-potential-difference nonlinear resistor.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] In recent years, in the field of the electronic equipment adopted as a transmitter etc., a miniaturization and integration are progressing quickly. Moreover, reduction-ization of the withstand voltage by the densification of IC is demanded, and the protection component and circuit design for preventing the destruction and malfunction of IC circuit by invasion of a high-voltage nature noise in connection with this are needed. The varistor which has electrical-potential-difference non-linear characteristics as such a protection component is adopted. In order to apply this varistor to IC circuit, conditions, such as that a control electrical potential difference is low, that electrostatic capacity is small, and a still smaller thing, are required. However, in the above-mentioned varistor, since voltage at reference current must be lowered to lowering a control electrical potential difference, there is a problem that electrostatic capacity becomes large. Moreover, although it is possible by making an electrode surface product small to lower electrostatic capacity, when it does in this way, there is a problem that a surge tolerated dose falls. The chip varistor of a laminating mold is conventionally proposed as what can respond to a miniaturization, reducing such a control electrical potential difference and electrostatic capacity (for example, refer to JP,58-23921,B). . This laminating mold varistor carries out the laminating of a semiconductive-ceramics layer and the internal electrode by turns, really sinters them, exposes the end side of the above-mentioned internal electrode to the both-ends side of this sintered compact, forms the external electrode connected to this both-ends side in the end side of the above-mentioned internal electrode, and is constituted. By the way, although the above-mentioned chip varistor is useful as a noise absorption component, when size of this varistor component is made small, there is a problem of being easy to produce surface current and the leakage current by surface discharge. Moreover, since Ag is used for the above-mentioned external electrode, in case a surface mount is carried out by soldering, there is a problem of being easy to produce solder ******. In order to avoid such the leakage current and solder ******, it is effective to coat and insulation-ize glass membrane to the outside surface except the external electrode of a sintered compact. As an approach of coating this glass membrane, the method of the above-mentioned glass being burned at the temperature of 400 - 900 **, and making the surface part of a sintered compact diffuse this glass is adopted conventionally. While being able to control the leakage current by forming this glass membrane, the plating film by electrolytic plating can be covered on the front face of an external electrode, and solder ****** can be prevented. Here, when covering the plating film to the above-mentioned external electrode, since the above-mentioned sintered compact is a semi-conductor, if the front face of this sintered compact is not insulation-ized certainly, it has a possibility that plating may grow up to be the whole front face, and may short-circuit, or the depressor effect of the leakage current may decrease. Therefore, it needs to equalize this thickness, therefore sets up the baking temperature of the above-mentioned glass highly, and is made to enlarge surface diffusion while a certain amount of thickness is required for the above-mentioned glass membrane.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EFFECT OF THE INVENTION

[Effect of the Invention] Since the free electrode which is not connected to an external electrode was arranged between the surface part of a sintered compact, and the internal electrode according to the chip mold varistor which starts this invention as mentioned above, it is effective in being able to equalize thickness, being burned in the case of forming glass membrane on the surface of a sintered compact, and making delicate control of temperature unnecessary, and controlling the diffusion to an internal electrode, and being able to prevent the bad influence to a varistor property.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, in the above-mentioned conventional chip varistor, when baking temperature of glass is made high, it may become active, this glass may attain even an internal electrode, as a result, voltage at reference current and a control electrical potential difference rise, and the grain boundary diffusion of glass also has the trouble of having a bad influence on a varistor property. In order to avoid the diffusion to an internal electrode here, making thickness of glass membrane into homogeneity, it is possible a glass content and by being burned and controlling temperature delicately. However, this control is very difficult and difficult in the present condition. It aims at offering the chip mold varistor which this invention was made in view of the above-mentioned conventional situation, and it can equalize thickness, being burned in the case of forming glass membrane on the surface of a sintered compact, and making delicate control of temperature unnecessary, and controls the diffusion to an internal electrode, and can prevent the bad influence to a varistor property.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

MEANS

[Means for Solving the Problem] Then, invention of claim 1 lays two or more internal electrodes under the interior of a sintered compact, and it is characterized by to arrange the free electrode which is not connected to the above-mentioned external electrode between the surface part of the above-mentioned sintered compact, and an internal electrode at the outside surface of the above-mentioned sintered compact in the chip mold varistor which comes to carry out covering formation of the glass membrane while it connects this internal electrode to the external electrode formed in the both-ends side of the above-mentioned sintered compact. Moreover, the above-mentioned free electrode of invention of claim 2 is larger than the area of the property section in an internal electrode, and it is characterized by having covered this property section, and claim 3 is further characterized by the above-mentioned free electrode consisting of an Ag-Pd alloy or Pt.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

OPERATION

[Function] According to the chip mold varistor concerning invention of claim 1, since the free electrode was arranged between the surface part of a sintered compact, and the internal electrode, this free electrode will control diffusion inside glass, therefore even if it can be burned and sets up temperature highly, the diffusion to an internal electrode can be reduced, and aggravation of a varistor property can be avoided. Consequently, being burned and making delicate control of temperature unnecessary, thickly [thickness], uniform glass membrane can be formed and insulation can be improved. Moreover, in invention of claim 2, since the free electrode was made larger than the area of the property section of an internal electrode, diffusion of the glass to an internal electrode can be controlled still more certainly. Furthermore, by invention of claim 3, since a silver-palladium alloy and platinum were adopted as the free electrode, the depressor effect of diffusion of glass can be improved.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example] Hereafter, the example of this invention is explained about drawing. Drawing 1 thru/or drawing 4 are drawings for explaining the chip mold varistor by one example of this invention. While laying underground the internal electrodes 3 and 3 of a pair which 1 is the chip mold varistor of this example in drawing, and become the interior of the sintered compact 2 of the shape of a rectangular parallelepiped which consists of semiconductive ceramics with which this uses ZnO as a principal component from an Ag-Pd alloy, it is the left of this sintered compact 2, The external electrode 4 which becomes right end side 2a and 2b from Ag is formed, and it is constituted. End side 3a of each above-mentioned internal electrode 3 is the left of the above-mentioned sintered compact 2, It exposes to right end side 2a and 2b by turns, and connects with the above-mentioned external electrode 4, and other end faces are enclosed in the sintered compact 2. Moreover, nickel plating film 8 by electrolytic plating is covered by the outside surface of the above-mentioned external electrode 4.
[0007] Moreover, the ceramic layer 5a part pinched with both the internal electrodes 3 of the above-mentioned sintered compact 2 serves as the property section A which discovers electrical-potential-difference non-linear characteristics, and this property section A serves as an opposed face of both the above-mentioned internal electrodes 3. Moreover, parts other than ceramic layer 5a of the above-mentioned sintered compact 2 serve as the ceramic layers 5b and 5c as a dummy.
[0008] Furthermore, glass membrane 6 is formed in the outside surface of the above-mentioned sintered compact 2, and this glass membrane 6 makes the surface part of a sintered compact 2 diffuse HOU lead silicate system glass powder by the ability being burned at an elevated temperature, and is formed.
[0009] And in ceramic layer 5b between the internal electrode 3 of the above-mentioned sintered compact 2, and a front face, and 5c, the free electrode 7 which consists of an Ag-Pd alloy which is not connected to the external electrode 4 is arranged, and this free electrode 7 is enclosed in the sintered compact 2. Moreover, this free electrode 7 is set up more greatly than the area of the property section A of the above-mentioned internal electrode 3, and has covered this property section A. Diffusion inside the above-mentioned glass layer 7 is controlled with this free electrode 7.
[0010] Next, the manufacture approach of the chip mold varistor 1 of this example is explained. first -- as a ceramic raw material -- ZnO of 99% or more of purity, Bi 2O3, CoCO3, MnO2, and Sb 2O3 98mol %, 0.5mol %, 0.5mol %, 0.5mol %, and 0.5 mol % come out comparatively, respectively, weighing capacity is carried out, pure water is added to this, it mixes with a ball mill for 24 hours, and a slurry is formed. Next, after carrying out filtration desiccation and corning this slurry, temporary baking is carried out at the temperature of 800 degrees C for 2 hours. Then, after adding pure water to this, pulverizing by BORUMIRU, after carrying out coarse grinding of this baking object with a pulverizer, and carrying out filtration desiccation of this, with an organic binder, it distributes in a solvent and a slurry is formed. this slurry to a doctor blade method -- 50 micrometers in thickness a green sheet -- forming -- this green sheet -- the magnitude of a predetermined dimension -- piercing -- many -- the ceramic sheet of several sheets is formed. Ceramic layer 5a which discovers electrical-potential-difference non-linear characteristics by this, and the ceramic layers 5b and 5c as a dummy are formed.
[0011] Next, the conductive paste which consists of an Ag-Pd alloy (7:3 comparatively) is created, this

paste is screen-stenciled on the top face of the above-mentioned ceramic layers 5a and 5c, and an internal electrode 3 is formed. In this case, it forms so that only end side 3a of an internal electrode 3 may be located in the rim of the ceramic layers 5a and 5c and the remaining end face may be located inside the ceramic layers 5a and 5c. Moreover, similarly conductive paste is printed on the top face of another ceramic layers 5b and 5c, and the free electrode 7 is formed in it. All the end faces of this are located inside the periphery of the ceramic layers 5b and 5c, and this free electrode 7 is formed so that it may become larger than the area of the property section A of the above-mentioned internal electrode 3.
[0012] Subsequently, end side 3a of each internal electrode 3 is the left so that each internal electrode 3 may counter on both sides of ceramic layer 5a, as shown in drawing 4 , It piles up so that it may be alternately located in the right, and the ceramic layers 5b and 5c which are not printed at all by the top face of this and the inferior surface of tongue are piled up two sheets. While piling up the ceramic layers 5b and 5c by which the free electrode 7 was furthermore formed in the top face of this, and the inferior surface of tongue, the ceramic layers 5b and 5c which are not printed at all are piled up two sheets. Next, the pressure of 2 t/cm2 is applied and stuck in the direction of a laminating of this by pressure, and this forms a layered product. Then, after cutting a layered product in a predetermined dimension, heating this at the temperature of 500 degrees C for 2 hours and vanishing a binder, a temperature up is carried out to 950 **, it calcinates for 2 hours, and a sintered compact 2 is obtained.
[0013] Thus, while holding the obtained sintered compact 2 in an alumina-ceramics pot, with a total weight [of the above-mentioned sintered compact / 1wt% of] HOU lead silicate system glass powder is added in this pot. And it heats to 700 - 900 **, rotating the above-mentioned porcelain pot. Then, the above-mentioned glass powder is spread into the surface part of a sintered compact 2, and, thereby, glass membrane 6 is formed. In this case, diffusion inside is prevented with the free electrode 8, osmosis in an internal electrode 3 will be controlled, and, as for glass powder, the glass membrane 6 of uniform thickness is formed in the surface part of a sintered compact 2.
[0014] Next, left where end side 3a of an internal electrode 3 of the above-mentioned sintered compact 2 was exposed, After applying Ag paste to right end side 2a and 2b, it heats for 10 minutes by 800 **, and the external electrode 4 is formed. After an appropriate time, electrolytic plating is performed to the above-mentioned sintered compact 2, and nickel plating film 8 is formed in the outside surface of the above-mentioned external electrode 4. In this case, since parts other than external electrode 4 of the above-mentioned sintered compact 2 are covered by glass membrane 6, plating does not adhere. Thereby, the chip mold varistor 1 of this example is manufactured.
[0015] Thus, since according to this example the free electrode 7 was arranged between the front face of a sintered compact 2, and the internal electrode 3 and the property section A of the above-mentioned internal electrode 3 was covered with this free electrode 7, diffusion of glass can be controlled with the free electrode 7, the diffusion to an internal electrode 3 is reduced, and the rise of discharge voltage and voltage at reference current can be avoided. Moreover, while being able to reduce the leakage current, without the tension of the fused glass being able to become small, being able to improve the wettability to a component, and being able to form the uniform glass membrane 6 thickly [thickness], consequently spoiling a surge tolerated dose and electrical-potential-difference depressor effect from the ability of temperature for it being burned and being made high, solder ****** at the time of soldering can be prevented. In addition, although the above-mentioned example explained taking the case of the structure which laid the internal electrode 3 of a pair underground in the sintered compact 2, this invention is not restricted to this and can be applied also to the thing of structure which laid many internal electrodes underground.
[0016]
[Table 1]

試料No.	電極材料	フリー電極パターン	Δt (mm)	ガラス熱処理温度 (℃)	バリスタ電圧 V_{1mA} (V)	非直線係数 α	静電容量 C (pF)	誘電損失 tan δ (%)	制限電圧比 V_{2A}/V_{1mA}	半田付 V_{1mA} 加工変化 (%)	電解Niメッキ後 V_{1mA} (V)	150 Aサージ変化率 ΔV_{1mA} (%)
1	Ag－Pd	なし	—	—	34.2	34	242	4.6	1.42	−63	Short	−10.7
2	↓	〃	—	700	34.1	34	243	4.7	1.43	−42	Short	−8.5
3	↓	〃	—	750	34.6	33	238	3.6	1.42	−39	Short	−9.1
4	↓	〃	—	800	35.0	31	218	2.6	1.45	−15	Short	−9.6
5	↓	〃	—	850	35.4	28	187	2.5	1.52	−10	35.3	−15.8
6	↓	〃	—	900	36.1	26	169	2.1	1.61	−5	36.1	−23.4
7	↓	b	0.2	850	34.9	28	192	2.8	1.45	−12	34.7	−8.6
8	↓	b	0.1	↓	34.6	28	201	3.0	1.45	−10	34.6	−6.5
9	↓	a	0.0	↓	34.4	30	225	3.1	1.42	−4	34.2	−2.4
10	↓	a	0.1	↓	34.4	33	235	2.9	1.41	−2	34.5	−1.8
11	↓	a	0.2	↓	34.3	34	244	3.0	1.42	−3	34.2	−1.5
12	↓	a	0.4	↓	34.2	34	246	3.2	1.41	−3	34.1	−1.6
13	↓	b	0.2	900	35.4	27	182	2.6	1.54	−9	35.5	−17.6
14	↓	b	0.1	↓	35.2	28	196	2.8	1.50	−6	35.3	−11.2
15	↓	a	0.0	↓	34.8	30	216	3.0	1.47	−4	34.6	−4.8
16	↓	a	0.1	↓	34.6	33	229	3.0	1.44	−3	34.4	−1.6
17	↓	a	0.2	↓	34.5	33	243	2.9	1.42	−4	34.5	−0.8
18	↓	a	0.4	↓	34.3	34	241	3.1	1.42	−2	34.3	−0.3
19	Pt	a	0.2	850	34.4	35	239	2.7	1.40	−3	34.4	−1.7
20	↓	a	↓	900	34.5	33	241	2.9	1.40	−2	34.4	−1.5

[0017] Table 1 shows the test result which checks the effectiveness of the chip mold varistor of this example and which went to accumulate. This trial created many chip mold varistors by the manufacture approach of the above-mentioned example, and measured the voltage at reference current at the time of changing the area of the free electrode in each of this varistor, a nonlinear multiplier, electrostatic capacity, electrostatic loss, a clamping voltage ratio, soldering processing rate of change, the voltage at reference current after plating, and surge rate of change, respectively. Moreover, as the above-mentioned

free electrode is shown in drawing 5 , property aspect product t1xt2 of an internal electrode are received (refer to drawing 5 (c)). When area of a free electrode was enlarged within the limits of t1+deltat and t2+deltat (0-0.4mm) (refer to drawing 5 (a)), and when area of a free electrode was made small within the limits of t1-deltat and t2-deltat (0.1 to 0.2 mm), it followed (refer to drawing 5 (b)). Here, to each sample after external electrode formation, the above-mentioned soldering processing rate of change was immersed in the 4x6 solder tub of 860 ** for 5 seconds using the rosin, after washing for 60 seconds by trichloroethane after this, was left for 1 hour and measured. Moreover, a clamping voltage ratio is 8x20microsec. It is the ratio of the output voltage/voltage at reference current when impressing a triangular current wave, and surge rate of change is the voltage at reference current/rate of the front [impression] varistor change of potential when leaving it for 1 hour, after impressing the above-mentioned triangular current wave. In addition, in order to compare, measurement with the same said of the conventional chip varistor which is not arranging the free electrode was carried out. Although it can be conventionally satisfied with a sample (No.1-6) of voltage at reference current and a nonlinear multiplier when [with glass baking temperature as low as 700 - 800 **] there is no free electrode so that clearly also from Table 1, in dielectric loss and soldering processing rate of change, it is low, and further, it adhered on the surface of [whole] the sintered compact, and short-circuits in plating processing, and the thickness of glass membrane serves as an ununiformity. Moreover, although it can be burned, and glass membrane is homogeneity when temperature is as high as more than 850 **, voltage at reference current and a nonlinear multiplier have deteriorated, and glass is spread even in the internal electrode. voltage at reference current on the other hand since glass turned around the free electrode and is spread inside, when the area of the above-mentioned free electrode is smaller than the property section of an internal electrode (sample No.7, 8, 13, 14), and a ratio -- in properties, such as a straight-line multiplier, effectiveness is small a little. On the other hand, the property which can be satisfied in soldering processing rate of change, the voltage at reference current after plating, and all the surge rate of change is acquired, without each spoiling each property of voltage at reference current, a nonlinear multiplier and dielectric loss, and a clamping voltage ratio, when area of a free electrode is made larger than the property section (sample No.9-12, 15-20).

[0018]

[Table 2]

試料No.	ガラス焼付温度（℃）	x軸（μm）	y軸（μm）
2	700	20	15
3	750	40	30
4	800	100	70
5	850	200	150
6	900	350	250

[0019]

[Table 3]

試料No.	ガラス焼付温度（℃）	x軸（μm）	y軸（μm）
11	850	130	150
17	900	170	250

[0020] Table 2 and 3 elects a sample (No.2-6) and this example sample (No.11, 17) which arranged the free electrode conventionally which is not arranging the free electrode adopted as the above-mentioned trial, carries out cross-section polish of each sample, and shows the result of having investigated the diffusion length of the glass of this by the electron probe X-ray microanalyser (energy dispersion mold). This measured the diffusion length in the direction x axis of a laminating of a sintered compact 2, and the diffusion length in the rectangular direction y-axis of this laminating direction, as shown in drawing 2 . In addition, the distance from the front face of the sintered compact 2 in each above-mentioned sample to the free electrode 7 is 100. mum, The distance from a free electrode to an internal electrode is 100. mum Carrying out [and], the distance from the side edge side of a sintered compact to the side edge side of an internal electrode is 400. mum It carried out. If baking temperature required for insulation-izing by the sample without a free electrode is made into 850 **, glass has reached even the property section of an internal electrode conventionally, so that clearly also from each table. On the other hand, it turns out that glass did not reach an internal electrode even if it could be burned and raised temperature by this example sample to 900 **, but the free electrode has controlled diffusion inside glass.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

EXAMPLE

[Example] Hereafter, the example of this invention is explained about drawing. Drawing 1 thru/or drawing 4 are drawings for explaining the chip mold varistor by one example of this invention. While laying underground the internal electrodes 3 and 3 of a pair which 1 is the chip mold varistor of this example in drawing, and become the interior of the sintered compact 2 of the shape of a rectangular parallelepiped which consists of semiconductive ceramics with which this uses ZnO as a principal component from an Ag-Pd alloy, it is the left of this sintered compact 2, The external electrode 4 which becomes right end side 2a and 2b from Ag is formed, and it is constituted. End side 3a of each above-mentioned internal electrode 3 is the left of the above-mentioned sintered compact 2, It exposes to right end side 2a and 2b by turns, and connects with the above-mentioned external electrode 4, and other end faces are enclosed in the sintered compact 2. Moreover, nickel plating film 8 by electrolytic plating is covered by the outside surface of the above-mentioned external electrode 4.
[0007] Moreover, the ceramic layer 5a part pinched with both the internal electrodes 3 of the above-mentioned sintered compact 2 serves as the property section A which discovers electrical-potential-difference non-linear characteristics, and this property section A serves as an opposed face of both the above-mentioned internal electrodes 3. Moreover, parts other than ceramic layer 5a of the above-mentioned sintered compact 2 serve as the ceramic layers 5b and 5c as a dummy.
[0008] Furthermore, glass membrane 6 is formed in the outside surface of the above-mentioned sintered compact 2, and this glass membrane 6 makes the surface part of a sintered compact 2 diffuse HOU lead silicate system glass powder by the ability being burned at an elevated temperature, and is formed.
[0009] And in ceramic layer 5b between the internal electrode 3 of the above-mentioned sintered compact 2, and a front face, and 5c, the free electrode 7 which consists of an Ag-Pd alloy which is not connected to the external electrode 4 is arranged, and this free electrode 7 is enclosed in the sintered compact 2. Moreover, this free electrode 7 is set up more greatly than the area of the property section A of the above-mentioned internal electrode 3, and has covered this property section A. Diffusion inside the above-mentioned glass layer 7 is controlled with this free electrode 7.
[0010] Next, the manufacture approach of the chip mold varistor 1 of this example is explained. first -- as a ceramic raw material -- ZnO of 99% or more of purity, Bi 2O3, CoCO3, MnO2, and Sb 2O3 98mol %, 0.5mol %, 0.5mol %, 0.5mol %, and 0.5 mol % come out comparatively, respectively, weighing capacity is carried out, pure water is added to this, it mixes with a ball mill for 24 hours, and a slurry is formed. Next, after carrying out filtration desiccation and coming this slurry, temporary baking is carried out at the temperature of 800 degrees C for 2 hours. Then, after adding pure water to this, pulverizing by BORUMIRU, after carrying out coarse grinding of this baking object with a pulverizer, and carrying out filtration desiccation of this, with an organic binder, it distributes in a solvent and a slurry is formed. this slurry to a doctor blade method -- 50 micrometers in thickness a green sheet -- forming -- this green sheet -- the magnitude of a predetermined dimension -- piercing -- many -- the ceramic sheet of several sheets is formed. Ceramic layer 5a which discovers electrical-potential-difference non-linear characteristics by this, and the ceramic layers 5b and 5c as a dummy are formed.
[0011] Next, the conductive paste which consists of an Ag-Pd alloy (7:3 comparatively) is created, this

paste is screen-stenciled on the top face of the above-mentioned ceramic layers 5a and 5c, and an internal electrode 3 is formed. In this case, it forms so that only end side 3a of an internal electrode 3 may be located in the rim of the ceramic layers 5a and 5c and the remaining end face may be located inside the ceramic layers 5a and 5c. Moreover, similarly conductive paste is printed on the top face of another ceramic layers 5b and 5c, and the free electrode 7 is formed in it. All the end faces of this are located inside the periphery of the ceramic layers 5b and 5c, and this free electrode 7 is formed so that it may become larger than the area of the property section A of the above-mentioned internal electrode 3.
[0012] Subsequently, end side 3a of each internal electrode 3 is the left so that each internal electrode 3 may counter on both sides of ceramic layer 5a, as shown in drawing 4 , It piles up so that it may be alternately located in the right, and the ceramic layers 5b and 5c which are not printed at all by the top face of this and the inferior surface of tongue are piled up two sheets. While piling up the ceramic layers 5b and 5c by which the free electrode 7 was furthermore formed in the top face of this, and the inferior surface of tongue, the ceramic layers 5b and 5c which are not printed at all are piled up two sheets. Next, the pressure of 2 t/cm2 is applied and stuck in the direction of a laminating of this by pressure, and this forms a layered product. Then, after cutting a layered product in a predetermined dimension, heating this at the temperature of 500 degrees C for 2 hours and vanishing a binder, a temperature up is carried out to 950 **, it calcinates for 2 hours, and a sintered compact 2 is obtained.
[0013] Thus, while holding the obtained sintered compact 2 in an alumina-ceramics pot, with a total weight [of the above-mentioned sintered compact / 1wt% of] HOU lead silicate system glass powder is added in this pot. And it heats to 700 - 900 **, rotating the above-mentioned porcelain pot. Then, the above-mentioned glass powder is spread into the surface part of a sintered compact 2, and, thereby, glass membrane 6 is formed. In this case, diffusion inside is prevented with the free electrode 8, osmosis in an internal electrode 3 will be controlled, and, as for glass powder, the glass membrane 6 of uniform thickness is formed in the surface part of a sintered compact 2.
[0014] Next, left where end side 3a of an internal electrode 3 of the above-mentioned sintered compact 2 was exposed, After applying Ag paste to right end side 2a and 2b, it heats for 10 minutes by 800 **, and the external electrode 4 is formed. After an appropriate time, electrolytic plating is performed to the above-mentioned sintered compact 2, and nickel plating film 8 is formed in the outside surface of the above-mentioned external electrode 4. In this case, since parts other than external electrode 4 of the above-mentioned sintered compact 2 are covered by glass membrane 6, plating does not adhere. Thereby, the chip mold varistor 1 of this example is manufactured.
[0015] Thus, since according to this example the free electrode 7 was arranged between the front face of a sintered compact 2, and the internal electrode 3 and the property section A of the above-mentioned internal electrode 3 was covered with this free electrode 7, diffusion of glass can be controlled with the free electrode 7, the diffusion to an internal electrode 3 is reduced, and the rise of discharge voltage and voltage at reference current can be avoided. Moreover, while being able to reduce the leakage current, without the tension of the fused glass being able to become small, being able to improve the wettability to a component, and being able to form the uniform glass membrane 6 thickly [thickness], consequently spoiling a surge tolerated dose and electrical-potential-difference depressor effect from the ability of temperature for it being burned and being made high, solder ****** at the time of soldering can be prevented. In addition, although the above-mentioned example explained taking the case of the structure which laid the internal electrode 3 of a pair underground in the sintered compact 2, this invention is not restricted to this and can be applied also to the thing of structure which laid many internal electrodes underground.
[0016]
[Table 1]

試料 No.	電極材料	フリー電極パターン	Δt (mm)	ガラス熱処理温度 (℃)	バリスタ電圧 V_{1mA} (V)	非直線係数 α	静電容量 C (pF)	誘電損失 tan δ (%)	制限電圧比 V_{2A}/V_{1mA}	半田付 V_{1mA} 加工変化 (%)	電解Niメッキ後 V_{1mA} (V)	150 Aサージ変化率 ΔV_{1mA} (%)
1	Ag－Pd	なし	—	—	34.2	34	242	4.6	1.42	−63	Short	−10.7
2	↓	〃	—	700	34.1	34	243	4.7	1.43	−42	Short	−8.5
3	↓	〃	—	750	34.6	33	238	3.6	1.42	−39	Short	−9.1
4	↓	〃	—	800	35.0	31	216	2.6	1.45	−15	Short	−9.6
5	↓	〃	—	850	35.4	28	187	2.5	1.52	−10	35.3	−15.6
6	↓	〃	—	900	36.1	26	169	2.1	1.61	−5	36.1	−23.4
7	↓	b	0.2	850	34.9	28	192	2.8	1.45	−12	34.7	−8.6
8	↓	b	0.1	↓	34.6	28	201	3.0	1.45	−10	34.6	−6.5
9	↓	a	0.0	↓	34.4	30	225	3.1	1.42	−4	34.2	−2.4
10	↓	a	0.1	↓	34.4	33	235	2.9	1.41	−2	34.5	−1.8
11	↓	a	0.2	↓	34.3	34	244	3.0	1.42	−3	34.2	−1.5
12	↓	a	0.4	↓	34.2	34	246	3.2	1.41	−3	34.1	−1.6
13	↓	b	0.2	900	35.4	27	182	2.6	1.54	−9	35.5	−17.6
14	↓	b	0.1	↓	35.2	28	196	2.8	1.50	−6	35.3	−11.2
15	↓	a	0.0	↓	34.8	30	216	3.0	1.47	−4	34.6	−4.8
16	↓	a	0.1	↓	34.6	33	229	3.0	1.44	−3	34.4	−1.6
17	↓	a	0.2	↓	34.5	33	243	2.9	1.42	−4	34.5	−0.8
18	↓	a	0.4	↓	34.3	34	241	3.1	1.42	−2	34.3	−0.3
19	Pt	a	0.2	850	34.4	35	239	2.7	1.40	−3	34.4	−1.7
20	↓	a	↓	900	34.5	33	241	2.9	1.40	−2	34.4	−1.5

[0017] Table 1 shows the test result which checks the effectiveness of the chip mold varistor of this example and which went to accumulate. This trial created many chip mold varistors by the manufacture approach of the above-mentioned example, and measured the voltage at reference current at the time of changing the area of the free electrode in each of this varistor, a nonlinear multiplier, electrostatic capacity, electrostatic loss, a clamping voltage ratio, soldering processing rate of change, the voltage at reference current after plating, and surge rate of change, respectively. Moreover, as the above-mentioned

free electrode is shown in drawing 5 , property aspect product t1xt2 of an internal electrode are received (refer to drawing 5 (c)). When area of a free electrode was enlarged within the limits of t1+deltat and t2+deltat (0-0.4mm) (refer to drawing 5 (a)), and when area of a free electrode was made small within the limits of t1-deltat and t2-deltat (0.1 to 0.2 mm), it followed (refer to drawing 5 (b)). Here, to each sample after external electrode formation, the above-mentioned soldering processing rate of change was immersed in the 4x6 solder tub of 860 ** for 5 seconds using the rosin, after washing for 60 seconds by trichloroethane after this, was left for 1 hour and measured. Moreover, a clamping voltage ratio is 8x20microsec. It is the ratio of the output voltage/voltage at reference current when impressing a triangular current wave, and surge rate of change is the voltage at reference current/rate of the front [impression] varistor change of potential when leaving it for 1 hour, after impressing the above-mentioned triangular current wave. In addition, in order to compare, measurement with the same said of the conventional chip varistor which is not arranging the free electrode was carried out. Although it can be conventionally satisfied with a sample (No.1-6) of voltage at reference current and a nonlinear multiplier when [with glass baking temperature as low as 700 - 800 **] there is no free electrode so that clearly also from Table 1, in dielectric loss and soldering processing rate of change, it is low, and further, it adhered on the surface of [whole] the sintered compact, and short-circuits in plating processing, and the thickness of glass membrane serves as an ununiformity. Moreover, although it can be burned, and glass membrane is homogeneity when temperature is as high as more than 850 **, voltage at reference current and a nonlinear multiplier have deteriorated, and glass is spread even in the internal electrode. voltage at reference current on the other hand since glass turned around the free electrode and is spread inside, when the area of the above-mentioned free electrode is smaller than the property section of an internal electrode (sample No.7, 8, 13, 14), and a ratio -- in properties, such as a straight-line multiplier, effectiveness is small a little. On the other hand, the property which can be satisfied in soldering processing rate of change, the voltage at reference current after plating, and all the surge rate of change is acquired, without each spoiling each property of voltage at reference current, a nonlinear multiplier and dielectric loss, and a clamping voltage ratio, when area of a free electrode is made larger than the property section (sample No.9-12, 15-20).

[0018]

[Table 2]

試料No.	ガラス焼付温度 (℃)	x軸 (μm)	y軸 (μm)
2	700	20	15
3	750	40	30
4	800	100	70
5	850	200	150
6	900	350	250

[0019]

[Table 3]

試料No.	ガラス焼付温度 (℃)	x軸 (μm)	y軸 (μm)
11	850	130	150
17	900	170	250

[0020] Table 2 and 3 elects a sample (No.2-6) and this example sample (No.11, 17) which arranged the free electrode conventionally which is not arranging the free electrode adopted as the above-mentioned trial, carries out cross-section polish of each sample, and shows the result of having investigated the diffusion length of the glass of this by the electron probe X-ray microanalyser (energy dispersion mold). This measured the diffusion length in the direction x axis of a laminating of a sintered compact 2, and the diffusion length in the rectangular direction y-axis of this laminating direction, as shown in drawing 2 . In addition, the distance from the front face of the sintered compact 2 in each above-mentioned sample to the free electrode 7 is 100. mum, The distance from a free electrode to an internal electrode is 100. mum Carrying out [and], the distance from the side edge side of a sintered compact to the side edge side of an internal electrode is 400. mum It carried out. If baking temperature required for insulation-izing by the sample without a free electrode is made into 850 **, glass has reached even the property section of an internal electrode conventionally, so that clearly also from each table. On the other hand, it turns out that glass did not reach an internal electrode even if it could be burned and raised temperature by this example sample to 900 **, but the free electrode has controlled diffusion inside glass.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the I-I line sectional view of drawing 3 for explaining the chip mold varistor by one example of this invention.
[Drawing 2] II-II of drawing 3 of the chip mold varistor of the above-mentioned example It is a line sectional view.
[Drawing 3] It is the perspective view of the chip mold varistor of the above-mentioned example.
[Drawing 4] It is the decomposition perspective view of the chip mold varistor of the above-mentioned example.
[Drawing 5] It is the top view of the free electrode for explaining the test method which checks the effectiveness of the above-mentioned example and which went to accumulate, and an internal electrode.
[Description of Notations]
1 Chip Mold Varistor
2 Sintered Compact
2a, 2b Left of a sintered compact, Right end side
3 Internal Electrode
3a The end side of an internal electrode
4 External Electrode
6 Glass Membrane
7 Free Electrode
A Property section

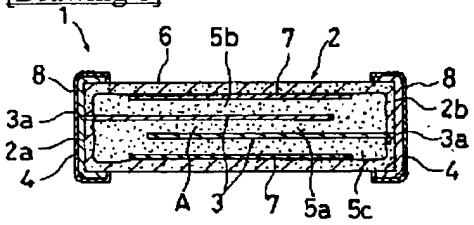
[Translation done.]

* NOTICES *

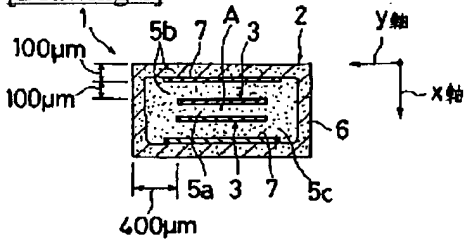
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

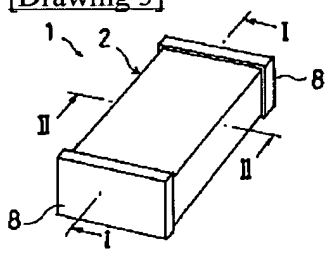
[Drawing 1]



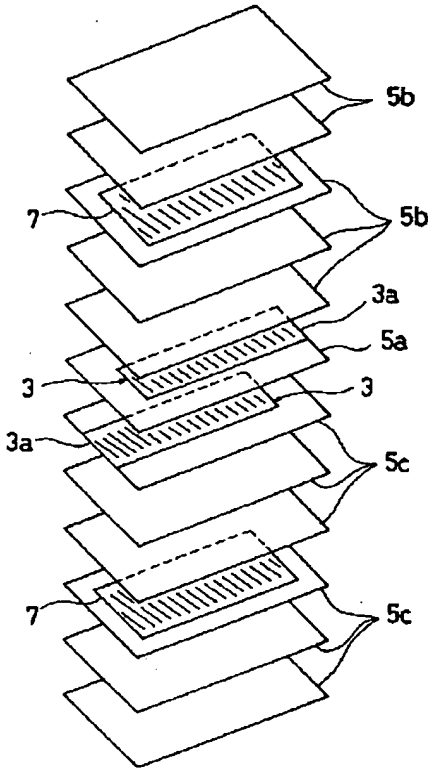
[Drawing 2]



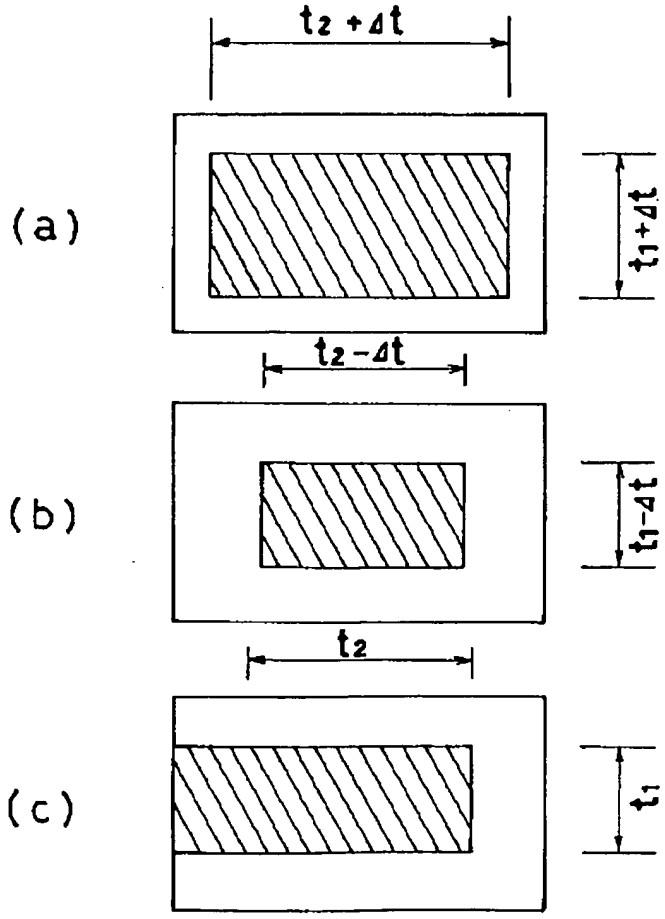
[Drawing 3]



[Drawing 4]



[Drawing 5]



[Translation done.]